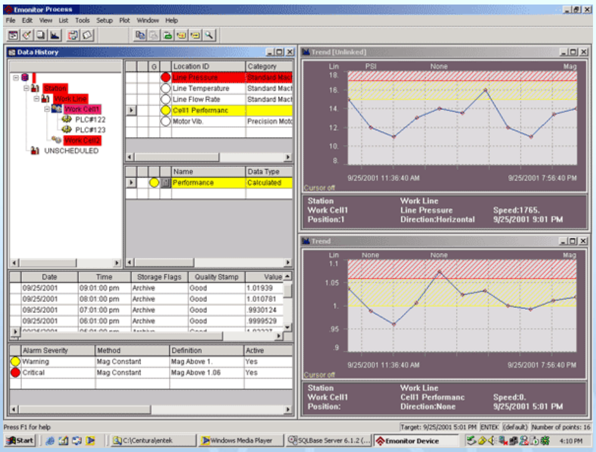
A/D Converters and Sampling Theorem

Department of Mechanical Engineering
Instructor: Jia-Yush Yen 3/31/2010

vision

What is a Physical Variable (I)

- You may like to do things like this



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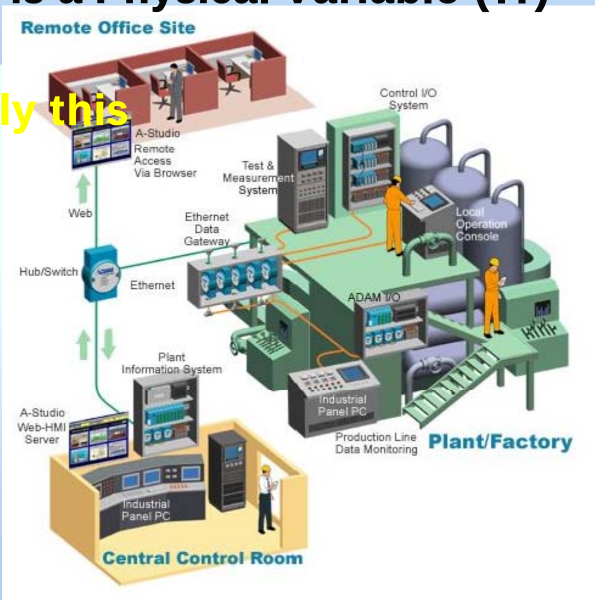
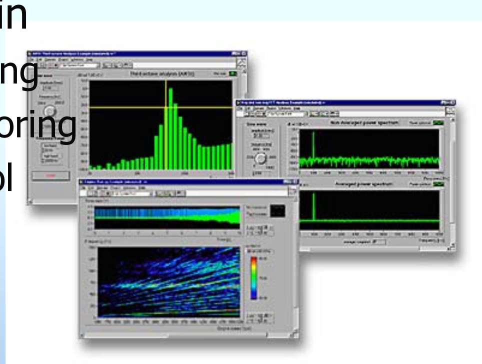
What is a Physical Variable (II)

- Or probably this



What is a Physical Variable (III)

- The physical properties that we are interested in
  - For studying
  - For monitoring
  - For control



What is a Physical Variable (IV)

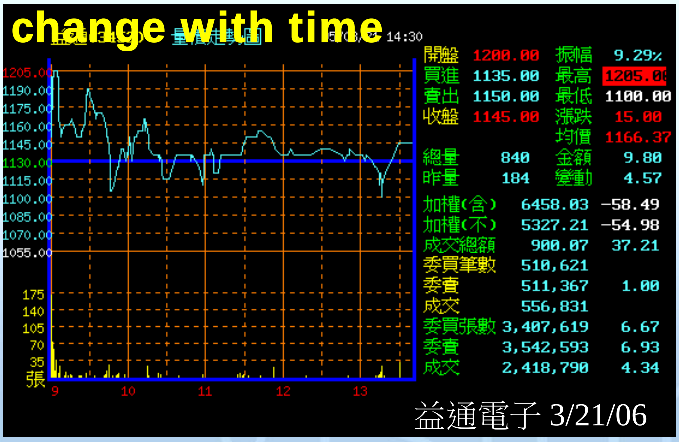
- Temperature
- Movement
- Vibration
- Speed
- Acceleration
- Sound pressure
- Heat flux
- …

The Time Variation of Physical Variables (I)

- You may say the temperature of the room is 25°C
- The stock price for MediaTek is 300 dollars
- The noise level near the MRT line is 80 dB
- The propulsion of Boeing 777 is 740,000 pound
- The Lamborghini Gallardo has got 500 horse-power

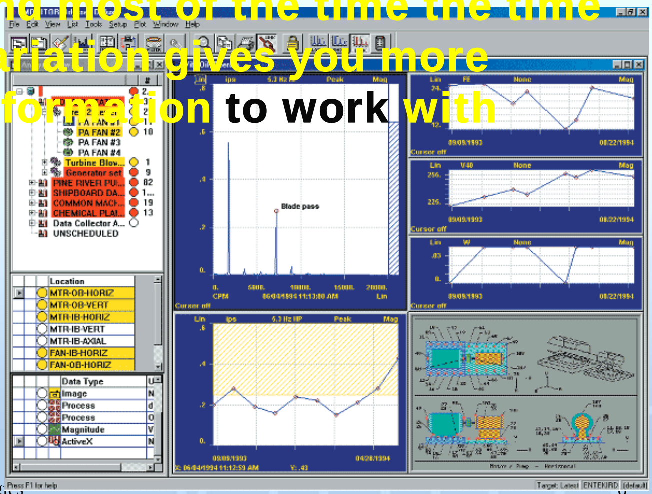
The Time Variation of Physical Variables (II)

- Eventually, these properties change with time



The Time Variation of Physical Variables (III)

- And most of the time the time variation gives you more information to work with



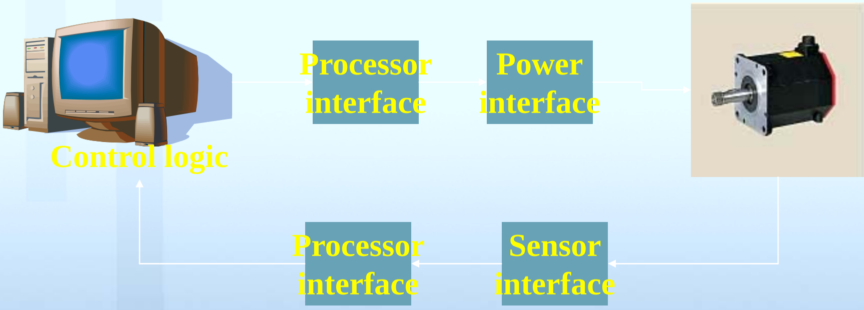
Outline

- Motivation
- The Acquisition System Setup
- The Physical Configuration of the Sampling System
- The Sampled Data
- The Appearance of the Sampled Data
- Sampling Consideration
- Aliasing
- Nyquist Sampling Theorem
- Various forms of A/D Hardware

Why Recording A Signal

- The time history of a physical variable allows you to
  - See the trend
  - Perform further data regression
    - Curve fit
    - Frequency spectrum
    - Wavelet transform
    - System identification
    - Control
    - …

How is Control Carried Out



How Is A Signal Recorded

- Computer only works with electrical signals
  - A sensor interface converts the signal into a easily handled **voltage change**
- Computer only works one instruction a time
  - A computer interface to **measure** the magnitude of the voltage **at some discrete instances**
- Computer only works with **numbers**

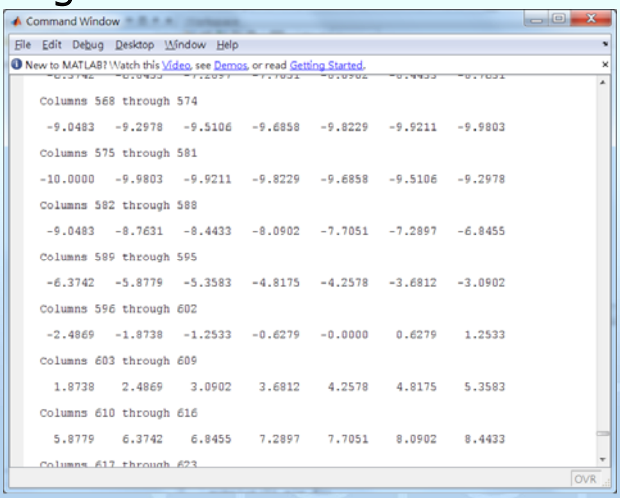
How is A Signal Recorded

- Computer only works with **numbers**
  - An interface to change the magnitudes into numbers (Preferably **integer numbers**)

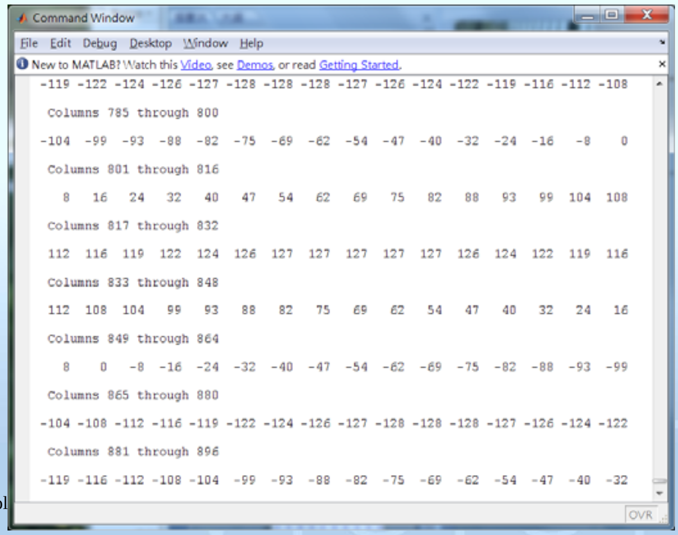
129
257
384
509
633
754
872
987
1097
1204
1305
1402
1493
1578
1657
1729
1795
1853

The Recorded Signal

- Floating Point Data



Actual Recorded 8-bit Data



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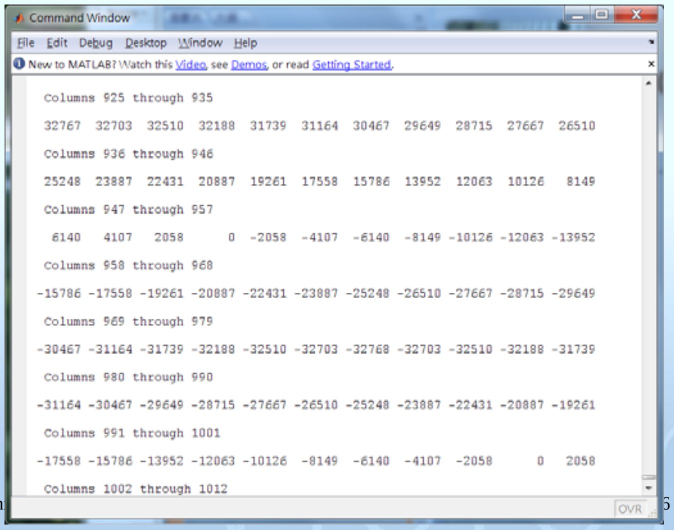
Recorded 16-bit Data



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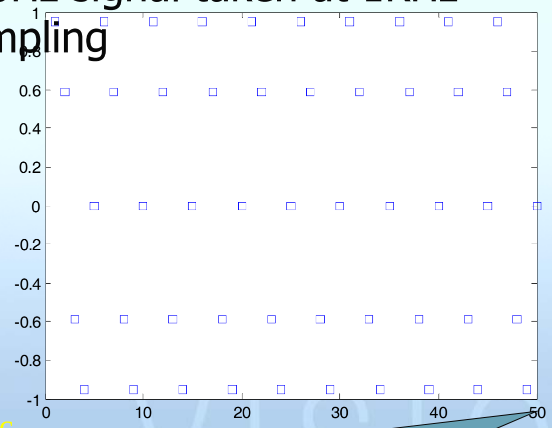
Signals as seen by a computer

- 200Hz signal taken at 1KHz sampling



1 KHz –
0.001 sec/sample
50 x 0.001 = 0.05 sec

What is the time stamp here?

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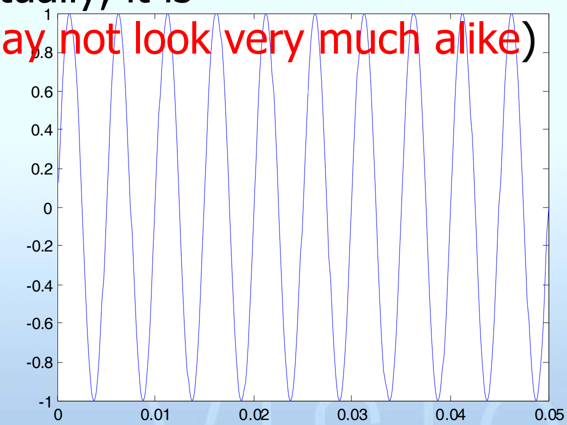
The original signal

- Actually, it is
(May not look very much alike)



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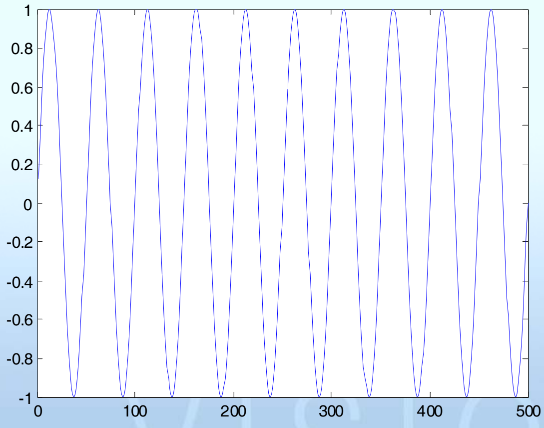
Suppose we do it faster

- Taken at 10KHz



0.0001 sec x 500
= 0.05 sec

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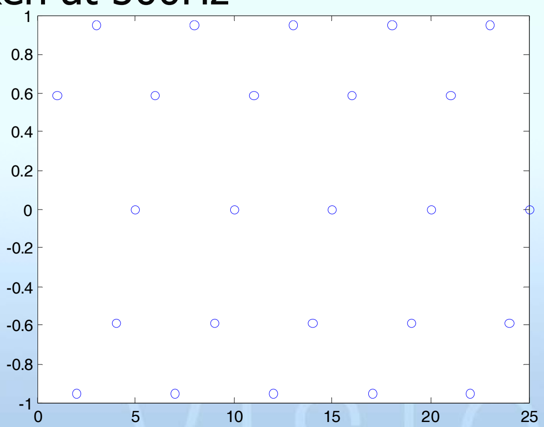
Suppose we do it slower

- Taken at 500Hz



0.002 x 25
= 0.05 sec

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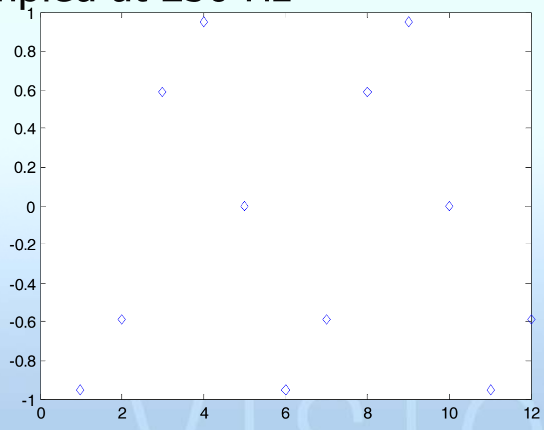
Suppose we do it even slower

- Sampled at 250 Hz



0.004 x 12
= 0.048 sec

How do we know we are looking at the right signal?

- We need many samples
  - How many?
- Many samples means fast rates
  - How fast?

Shannon Sampling Theorem

Reprinted with corrections from *The Bell System Technical Journal*,
Vol. 27, pp. 379–423, 623–656, July, October, 1948.

A Mathematical Theory of Communication

By C. E. SHANNON

INTRODUCTION

THE recent development of various methods of modulation such as PCM and PPM which exchange bandwidth for signal-to-noise ratio has intensified the interest in a general theory of communication. A basis for such a theory is contained in the important papers of Nyquist[1] and Hartley[2] on this subject. In the present paper we will extend the theory to include a number of new factors, in particular the effect of noise in the channel, and the savings possible due to the statistical structure of the original message and due to the nature of the final destination of the information.

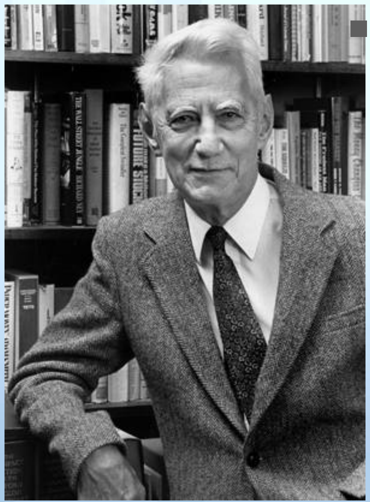
The fundamental problem of communication is that of reproducing at one point either exactly or approximately a message selected at another point. Frequently the messages have *meaning*; that is they refer to or are correlated according to some system with certain physical or conceptual entities. These semantic aspects of communication are irrelevant to the engineering problem. The significant aspect is that the actual message is one *selected from a set* of possible messages. The system must be designed to operate for each possible selection, not just the one which will actually be chosen since this is unknown at the time of design.

If the number of messages in the set is finite then this number or any monotonic function of this number can be regarded as a measure of the information produced when one message is chosen from the set, all choices being equally likely. As was pointed out by Hartley the most natural choice is the logarithmic function. Although this definition must be generalized considerably when we consider the influence of the statistics of the message and when we have a continuous range of messages, we will in all cases use an essentially logarithmic measure.

The logarithmic measure is more convenient for various reasons:

Shannon Sampling Theorem

- The **Nyquist–Shannon sampling theorem**, also known as **Whittaker–Shannon sampling theorem**, is a fundamental result in the field of information theory, in particular telecommunications.
  - In addition to E. T. Whittaker (statistical theorem published 1915), Claude Shannon and Harry Nyquist, it is also attributed to Kotelnikov, and sometimes referred to as, simply, the ***sampling theorem***.



- **Claude Elwood Shannon** (April 30, 1916 – February 24, 2001), an American electrical engineer and mathematician, has been called "the father of information theory", and was the founder of practical digital circuit design theory.

http://www.wikipedia.org

- **Edmund Taylor Whittaker** (24 October 1873 - 24 March 1956) was an English mathematician, who contributed widely to applied mathematics, mathematical physics and the theory of special functions. He had a particular interest in numerical analysis, but also worked on celestial mechanics and the history of applied mathematics and the history of physics. He was born in Southport, in Merseyside.

http://www.lms.ac.uk/newsletter/328/328_09.html

- **Harry Nyquist** (February 7, 1889 – April 4, 1976) was an important contributor to information theory.
- He was born in Nilsby, Sweden. He emigrated to the USA in 1907 and entered the University of North Dakota in 1912. He received a Ph.D. in physics at Yale University in 1917. He worked at AT&T from 1917 to 1934, then moved to Bell Telephone Laboratories.
- As an engineer at Bell Laboratories, he did important work on thermal noise ("Johnson-Nyquist noise") and the stability of feedback amplifiers.
- His early theoretical work on determining the bandwidth requirements for transmitting information, as published in "Certain factors affecting telegraph speed" (*Bell System Technical Journal*, 3, 324–346, 1924), laid the foundations for later advances by Claude Shannon, which led to the development of information theory.
- In 1927 Nyquist determined that an analog signal should be sampled at regular intervals over time and at twice the frequency of the signal's bandwidth in order to be converted into an adequate representation of the signal in digital form. Nyquist published his results in the paper *Certain topics in Telegraph Transmission Theory* (1928). This rule is now known as the Nyquist–Shannon sampling theorem.
- He retired from Bell Labs in 1954. Nyquist died in Harlingen, Texas on April 4, 1976.

Ref: en.wikipedia.org/wiki/Harry_Nyquist

Certain Topics in Telegraph Transmission Theory

H. NYQUIST, MEMBER, A. I. E. E.

Classic Paper

Synopsis—The most obvious method for determining the distortion of telegraph signals is to calculate the transients of the telegraph system. This method has been treated by various writers, and solutions are available for telegraph lines with simple terminal conditions. It is well known that the extension of the same methods to more complicated terminal conditions, which represent the usual terminal apparatus, leads to great difficulties.

The present paper attacks the same problem from the alternative standpoint of the steady-state characteristics of the system. This method has the advantage over the method of transients that the complication of the circuit which results from the use of terminal apparatus does not complicate the calculations materially. This method of treatment necessitates expressing the criteria of distortionless transmission in terms of the steady-state characteristics. Accordingly, a considerable portion of the paper describes and illustrates a method for making this translation.

A discussion is given of the minimum frequency range required for transmission at a given speed of signaling. In the case of carrier telegraphy, this discussion includes a comparison of single-sideband and double-sideband transmission. A number of incidental topics is also discussed.

SCOPE

THE purpose of this paper is to set forth the results of theoretical studies of telegraph systems which have been made from time to time. These results are naturally disconnected and in order to make a connected story it has been necessary to include a certain amount of material which is already well known to telegraph engineers. The following topics are discussed:

1) The required frequency band is directly proportional to the signaling speed.
2) A repeated telegraph signal (of any length) may be considered as being made up of sinusoidal components. When the amplitude and phase, or real and imaginary parts, of these components are plotted as ordinates with their frequencies as abscissas, and when the frequency axis is divided into parts each being a frequency band of width numerically equal to the speed of signaling, it is found that the information conveyed in any band is substantially identical with that conveyed in any other; and the bands may be said to be mutually redundant.
3) The minimum band width required for unambiguous interpretation is substantially equal, numerically, to the speed of signaling and is substantially independent of the number of current values employed.
4) A criterion of perfect transmission is selected; and a discussion is given of the characteristics which the received wave must have to be nondistorting with the requirement that the frequency range should not be greater than necessary.
5) Directions are sketched for specifying systems to meet this requirement.
6) Several alternative criteria of distortionless transmission are considered and a method for computing the corresponding transmission characteristics of the circuit is explained and illustrated.
7) An analysis is given of the carrier wave, and it is shown that the usual carrier telegraph requires twice as much frequency range as the corresponding d-c. telegraph, other things being equal.
8) A discussion is given of two alternative methods for overcoming this inefficiency of carrier telegraphy, namely, the use of phase discrimination and of a single sideband.
9) After the d-c. and carrier waves have thus been analyzed a corresponding analysis is given of an arbitrary wave shape, including these two as special cases. Calculations are given on the shaping of the transmitted wave so as to make the received wave perfect.
10) A discussion is given of the dual aspect of the telegraph wave. The wave may be looked on either as a function of ω, requiring the so-called steady-state method of treatment, or as a function of t requiring the so-called method of transients. It is shown that

This work was presented at the Winter Convention of the A. I. E. E., New York, NY, February 13–17, 1928. Reprinted from *Transactions of the A. I. E. E.*, pp. 617–644, Feb. 1928.

The author, deceased, was with the American Telephone and Telegraph Co., New York, NY.

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Shannon Sampling Theorem

- A signal that is bandlimited is constrained in terms of how fast it can change and therefore how much detail it can convey in between discrete moments of time.
- The sampling theorem means that the discrete samples are a complete representation of the signal if the bandwidth is less than half the sampling rate, which is referred to as the Nyquist frequency.
- Frequency components that are above the Nyquist frequency are subject to a phenomenon called aliasing, which is undesirable in most applications. The severity of the problem depends on the relative strength of the aliased components.

Shannon Sampling Theorem

Let $x(t)$ represent a real-valued continuous-time signal and let $X(f)$ represent its unitary Fourier transform (to the domain of ordinary frequency, Hz). I.e.:

$$X(f) = \Im\{x(t)\} = \int_{-\infty}^{\infty} x(t) e^{-j2\pi ft} dt$$

The right figure depicts a bandlimited $X(f)$ whose highest frequency is f_H. i.e.:

$$X(f) = 0 \text{ for } |f| > f_H$$

Then the condition for alias-free sampling at rate f_s (in samples per second) is:

$$f_s > 2f_H \quad \text{(Nyquist rate)}$$

or equivalently:

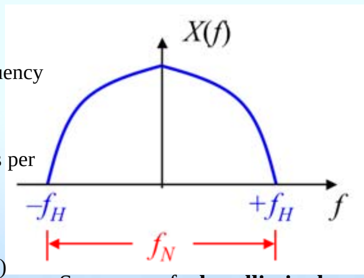
$$f_H < f_s/2 \quad \text{(Nyquist frequency)}$$

The time interval between successive samples is a constant, referred to as *sampling interval*. It is given, in seconds, by:

$$T = 1/f_s$$

And the samples of $x(t)$ are denoted by:

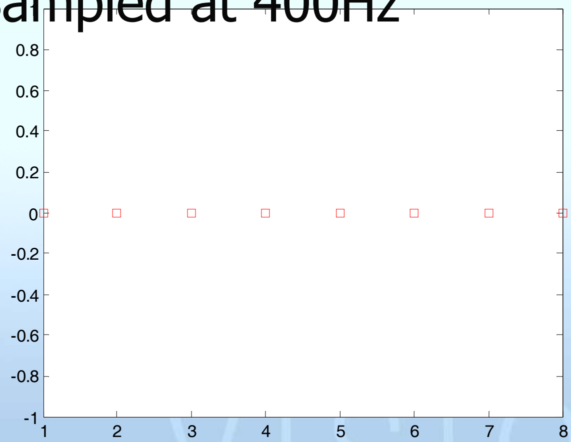
$$x(n/f_s) = x(nT),\ n \in Z$$



Spectrum of a **bandlimited signal** as a function of frequency

The same signal

- Sampled at 400Hz



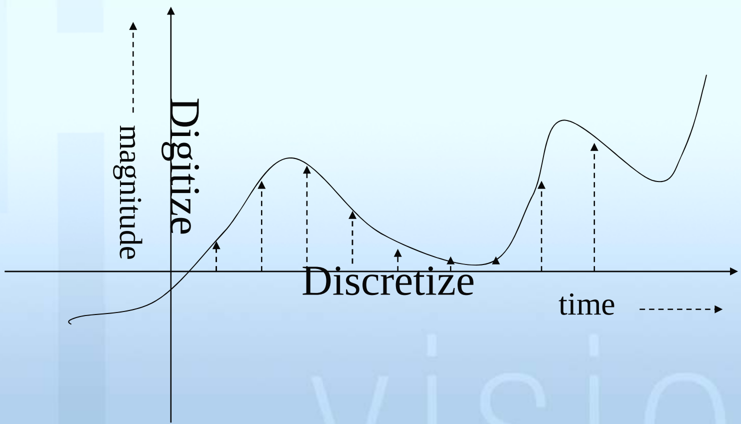
Digitizing a Signal

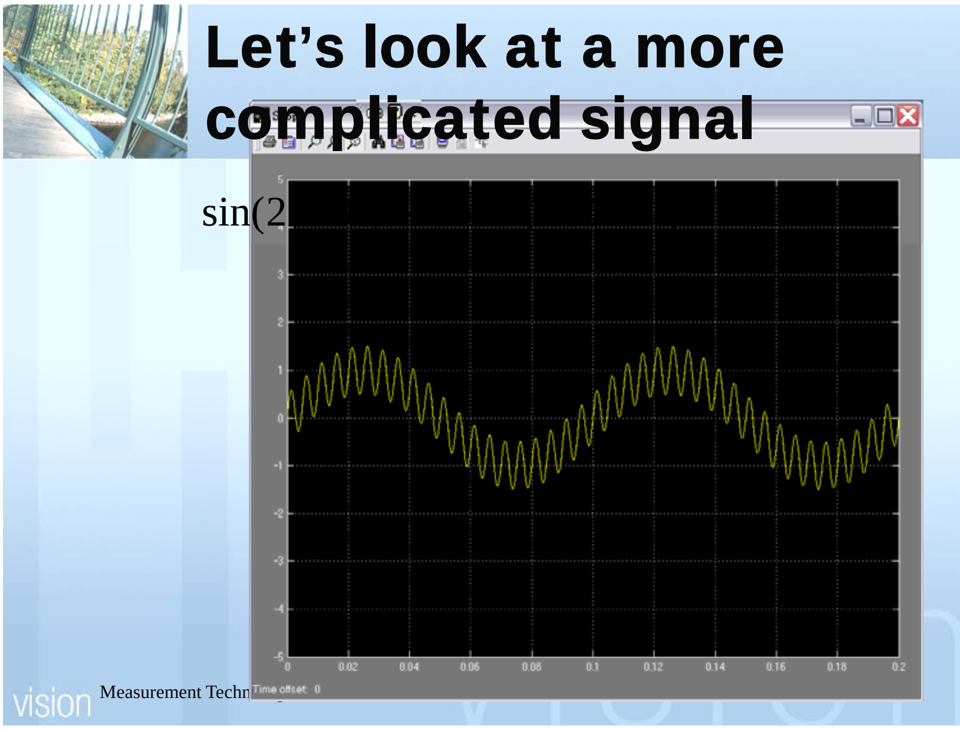
- The device to digitize a signal is called an "Analog-to-Digital (A/D) Converter"

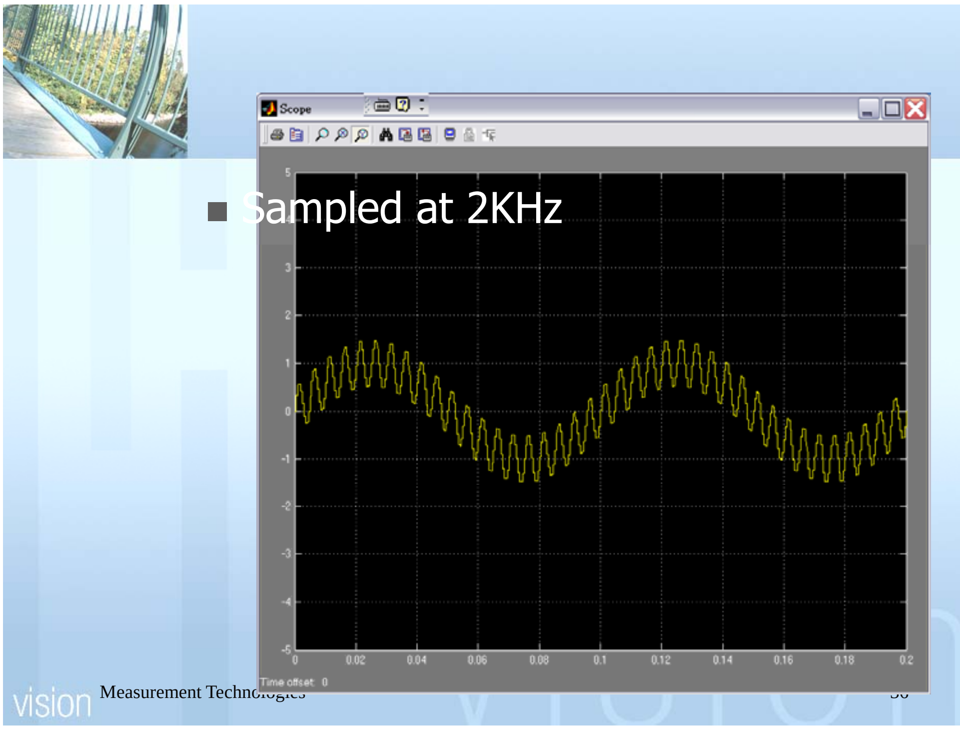
Concept of Sampling

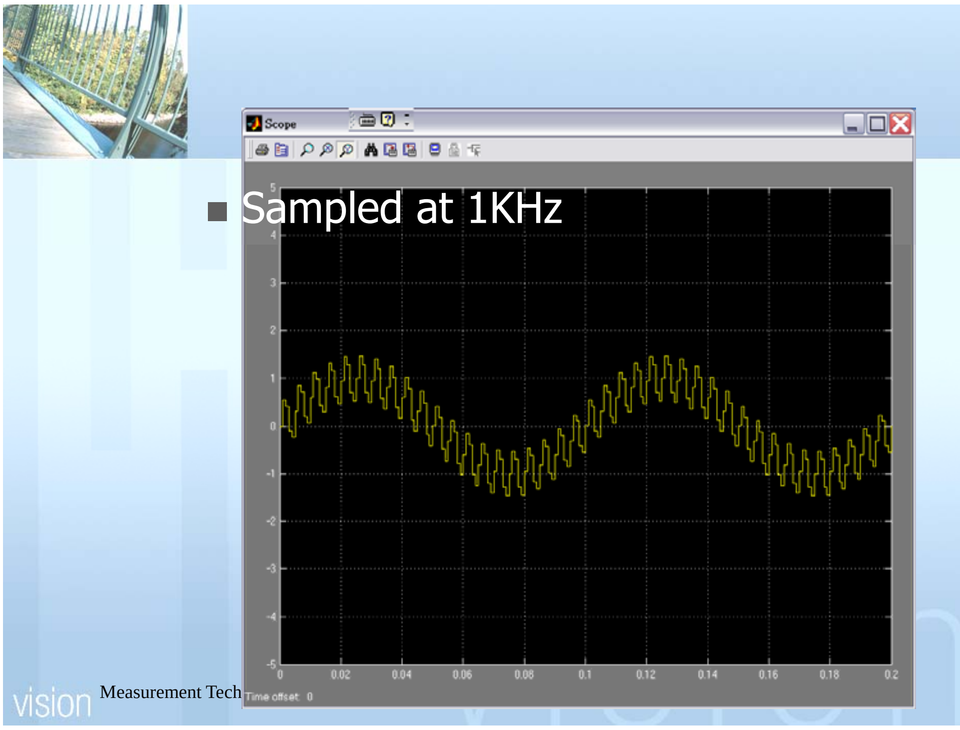
- You only take data at certain time instances
  - (There is no information about the signal in between samples.)

Discretize vs. Digitize

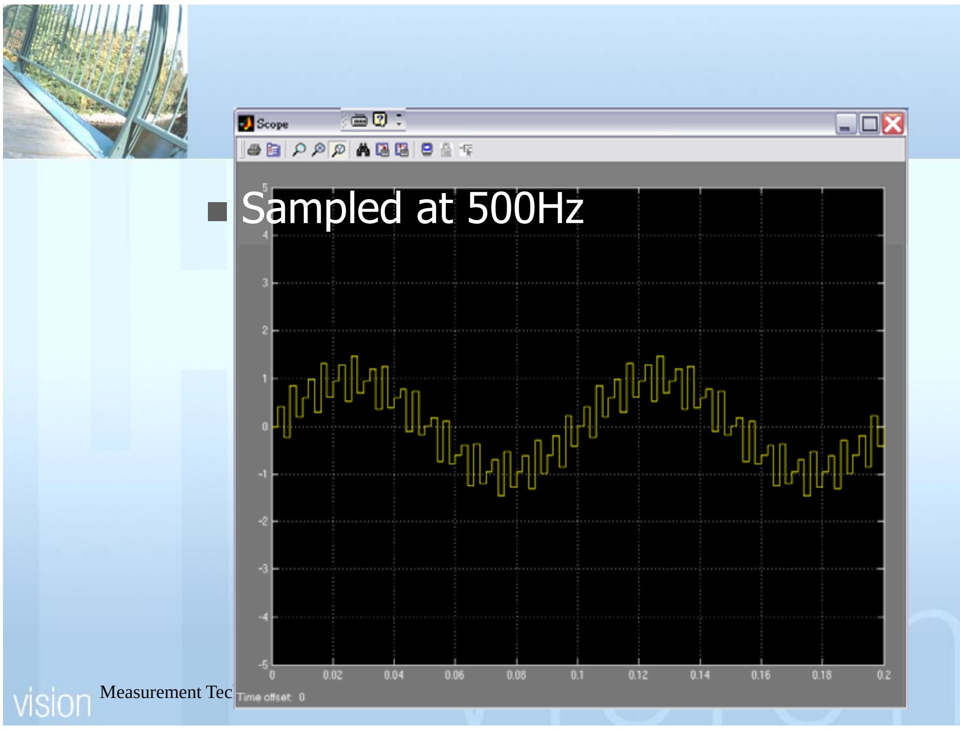



Let's look at a more complicated signal
sin(2
Measurement Techn
vision


Scope
Sampled at 2KHz
Measurement Technologies
vision

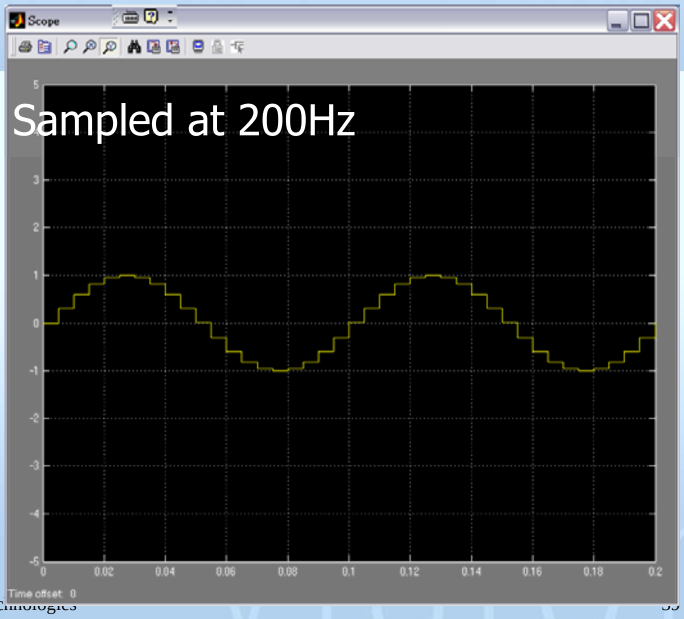


Sampled at 1KHz
Scope
Time offset: 0
vision
Measurement Tech

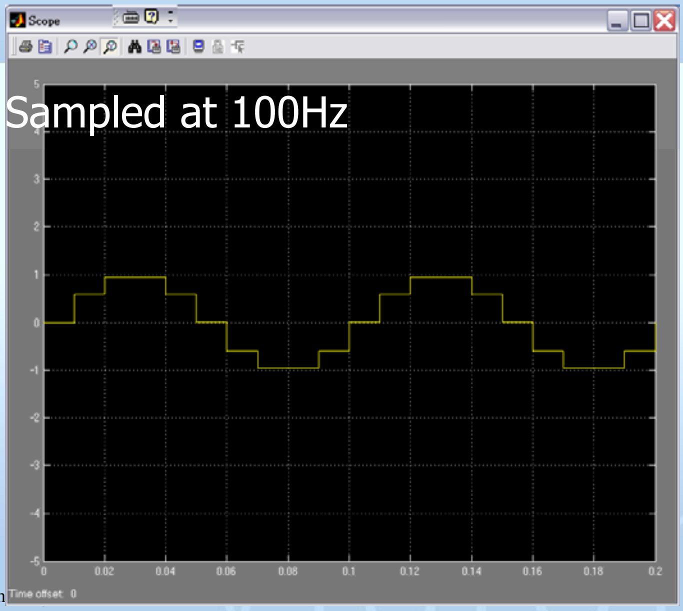


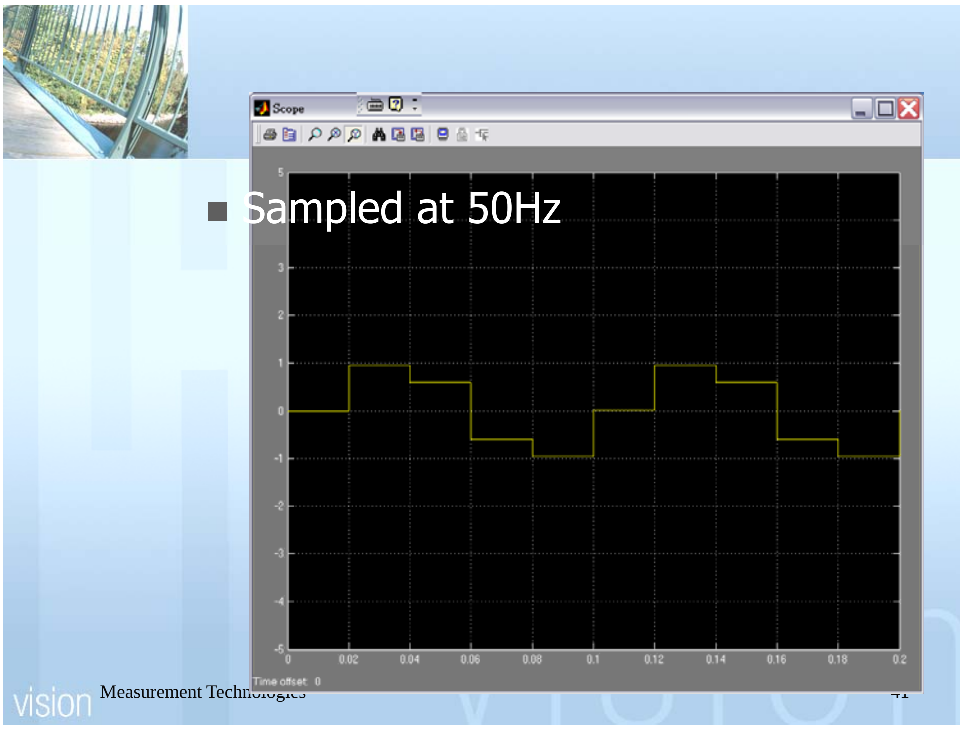
Sampled at 500Hz
Scope
Time offset: 0
vision
Measurement Tec

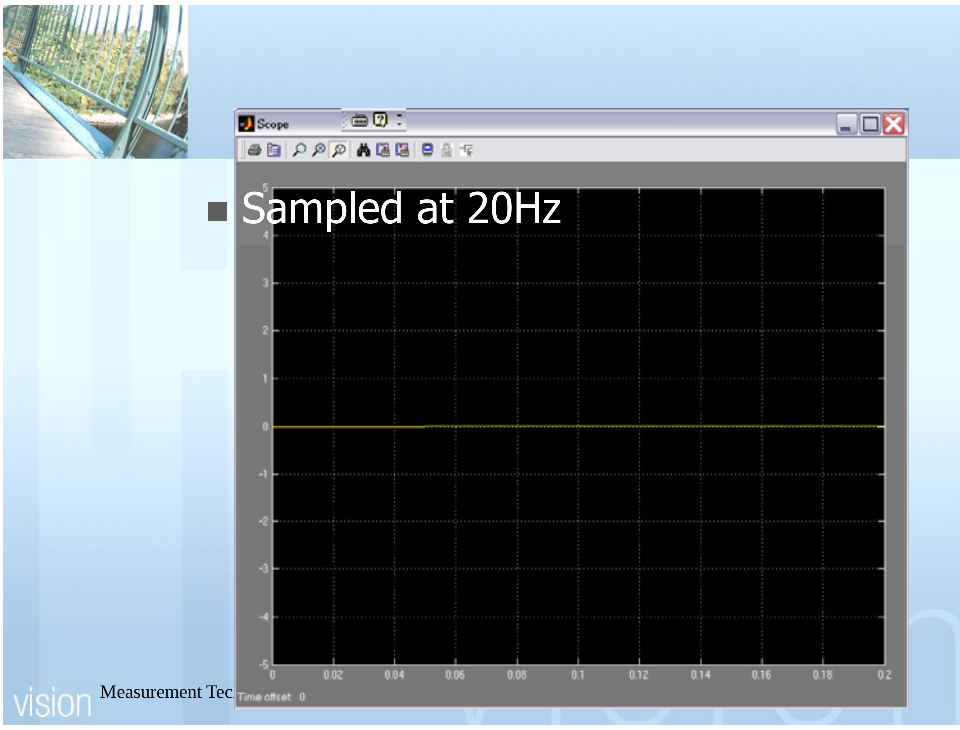
- Sampled at 200Hz

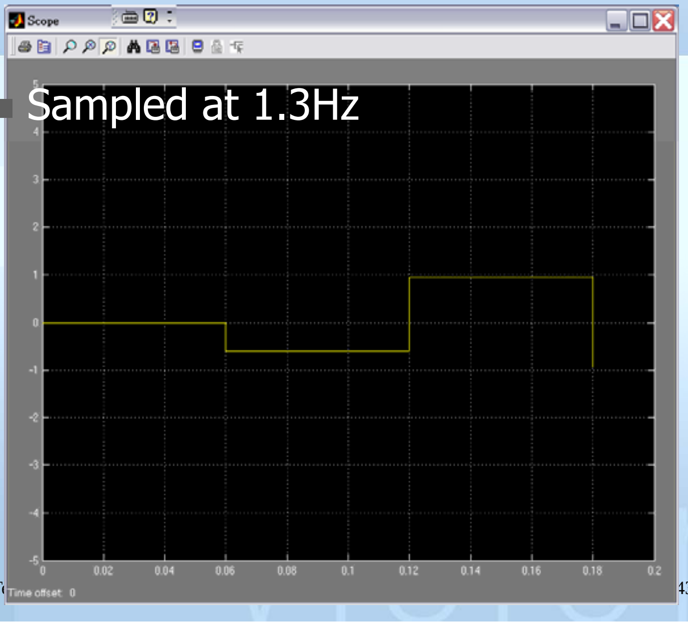


- Sampled at 100Hz



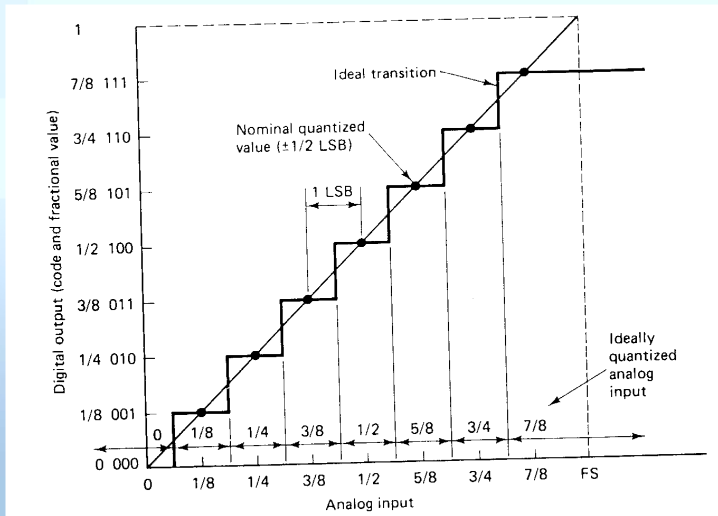

Sampled at 50Hz
Scope
Time offset: 0
vision
Measurement Technologies


Sampled at 20Hz
Scope
Time offset: 0
vision
Measurement Tec



- Sampled at 1.3Hz

Digitization



A/D Converter Characteristics

- Consider N-bit A/D converter
- The sampled data

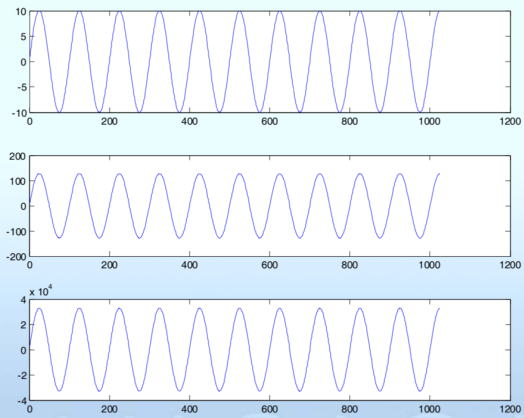
$$n = \left[\frac{V - V_{ref}^{-}}{\Delta V} + \frac{1}{2} \right]_{round}, \quad \Delta V = \frac{V_{ref}^{+} - V_{ref}^{-}}{2^N - 1}$$

In Other Word

- When sampling data
  - 1. Amplify the signal to $V_{ref}^{+} \leftrightarrow V_{ref}^{-}$ before attaching to A/D
  - 2. When recording – multiply data by *(in_data_array)*$*\Delta V$ to obtain the correct magnitude

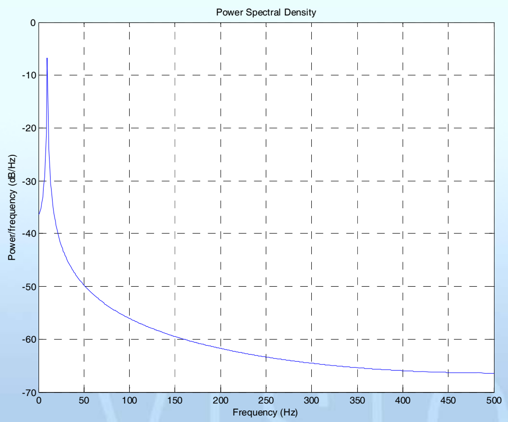
Effect of Bit-depth

- 1 Floating point
- 8 bits sampled
- 16 bits sampled



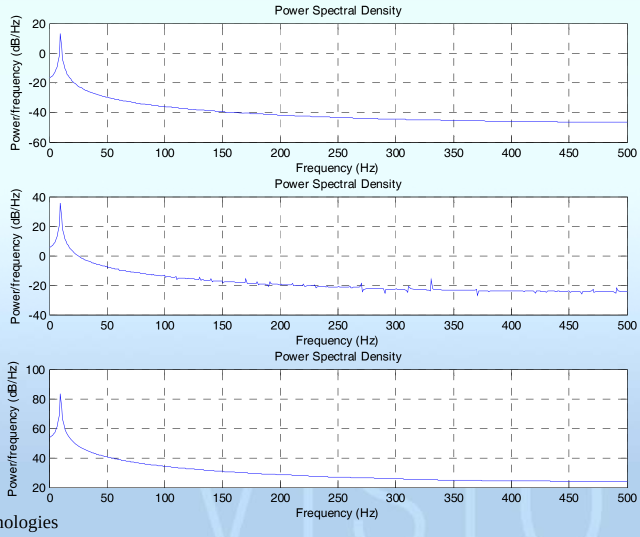
Power Spectrum Consideration

- Floating point signal



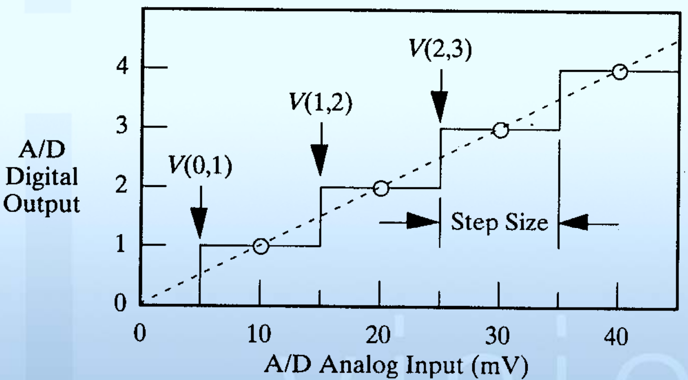
Compare Bit-length

- Floating
- 8-bit
- 16-bit



Sample-and-Hold

- Ideal response of an S/H

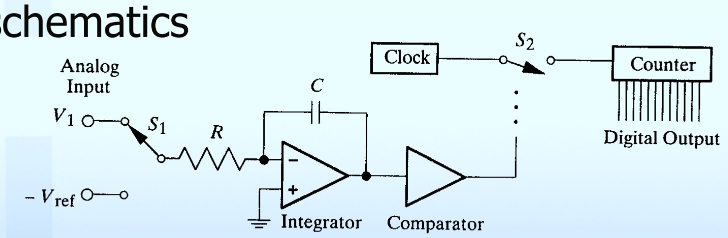


Analog-to-Digital Converter

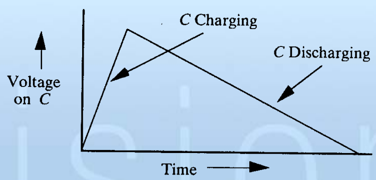
- Integrating Type (Charge-digitizing A/D)
- Tracking A/D
- Successive Approximation Type
- Flash A/D converter
- Subranging Flash A/D

Integrating A/D Converter

- Integrating dual-slop A/D converter schematics

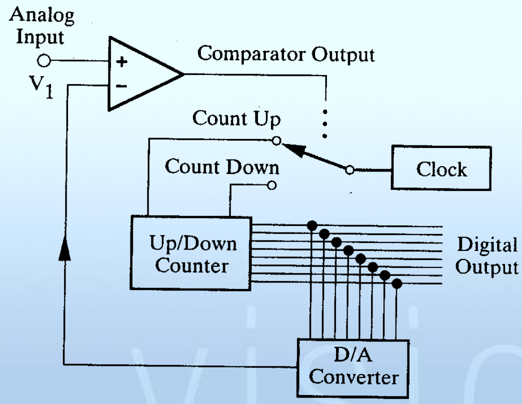


- Operating principle



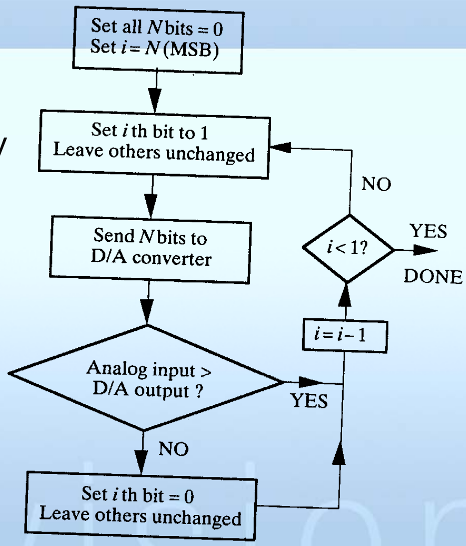
Tracking A/D Converter

- Repeatedly compares its input with the output of a D/A converter.



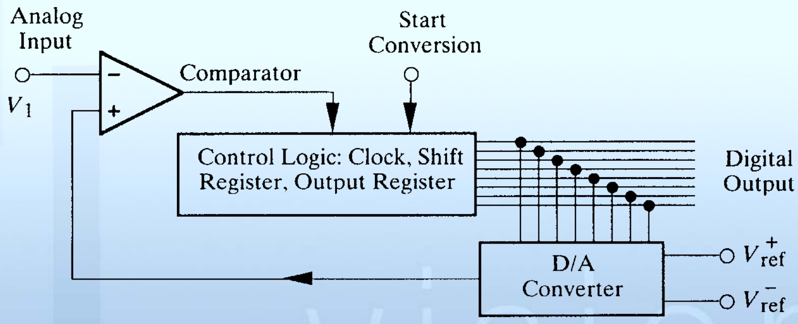
Successive Approximation A/D (I)

- Flow chart –
  - Uses a binary search to sequentially determine the bits of the output



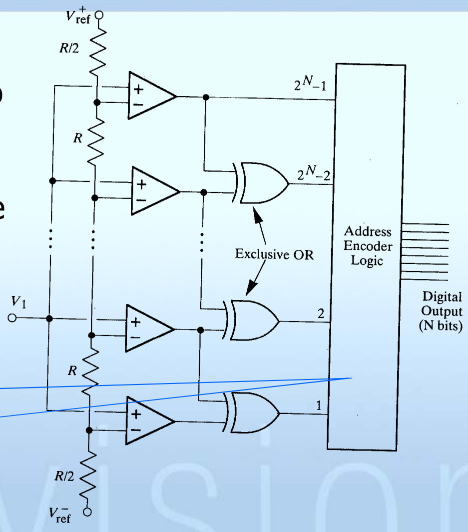
Successive Approximation A/D (II)

- Block diagram for the successive approximation A/D



Flash A/D Converter

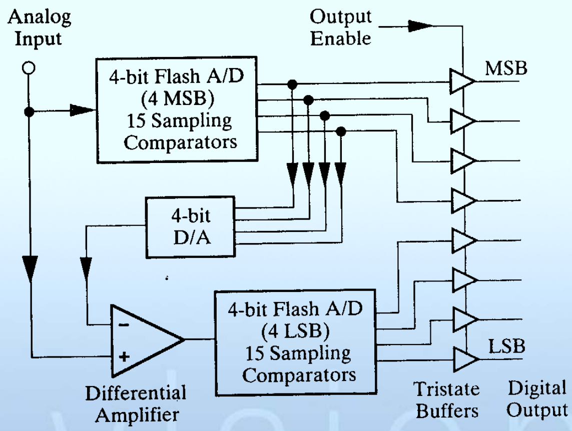
- Uses $2^N - 1$ comparators to determine simultaneously all N bits of the digital outputs.



Generates the address of the bit most representative to the input voltage

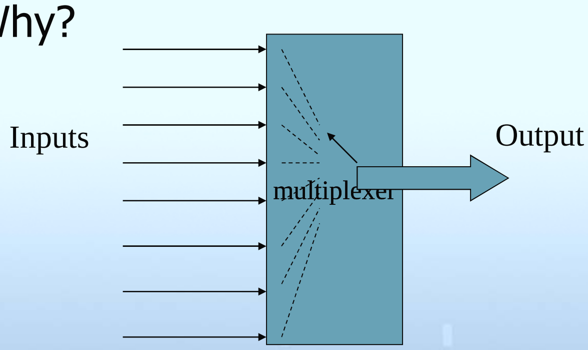
Subranging Flash A/D Converter

- Flash converter is too costly
- More practical solution
  - Hybrid between the successive-approximation and the flash converter



Multi-channel Consideration

- This would work "funny"
- Why?

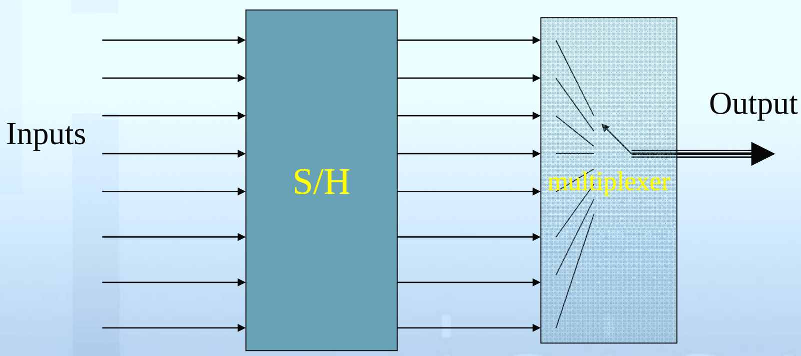


Conversion Time Consideration

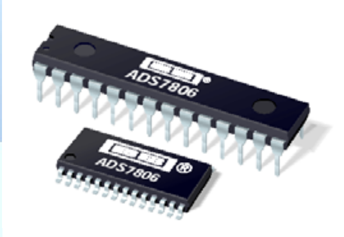
- Conversion takes time (especially integrating A/D)
- S/H needs time to settle
- Output digital data takes time (especially when using serial output)

Actually

- This is more ideal application



TI ADS7806



Ref: www.ti.com

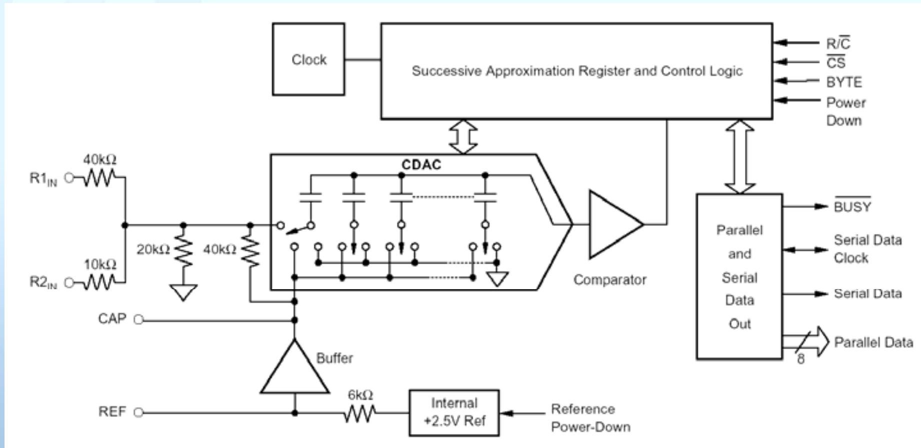
The ADS7806 is a low-power, 12-bit, sampling Analog-to-Digital (A/D) converter using state of the art CMOS structures.

It contains a complete 12-bit, capacitor-based, Successive Approximation Register (SAR) A/D converter with sample and-hold, clock, reference, and a microprocessor interface with parallel and serial output drivers.

The ADS7806 can acquire and convert to full 12-bit accuracy in 25μs max, while consuming only 35mW max. Laser trimmed scaling resistors provide standard industrial input ranges of ±10V and 0V to +5V. In addition, a 0V to +4V range allows development of complete single-supply systems.

The ADS7806 is available in a 0.3" DIP-28 and SO-28, both fully specified for operation over the industrial –40°C to +85°C temperature range.

ADS7806 – successive approximation



PIN DESCRIPTIONS

PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	$R1_{IN}$		Analog Input. See Figure 7.
2	AGND1		Analog Sense Ground
3	$R2_{IN}$		Analog Input. See Figure 7.
4	CAP		Reference Buffer Output. 2.2µF tantalum capacitor to ground.
5	REF		Reference Input/Output. 2.2µF tantalum capacitor to ground.
6	AGND2		Analog Ground
7	SB/$\overline{\text{BTC}}$	I	Selects Straight Binary or Binary Two's Complement for Output Data Format.
8	EXT/$\overline{\text{INT}}$	I	External/Internal data clock select.
9	D7	O	Data Bit 3 if BYTE is HIGH. Data bit 11 (MSB) if BYTE is LOW. Hi-Z when $\overline{\text{CS}}$ is HIGH and/or R/$\overline{\text{C}}$ is LOW. Leave unconnected when using serial output.
10	D6	O	Data Bit 2 if BYTE is HIGH. Data bit 10 if BYTE is LOW. Hi-Z when $\overline{\text{CS}}$ is HIGH and/or R/$\overline{\text{C}}$ is LOW.
11	D5	O	Data Bit 1 if BYTE is HIGH. Data bit 9 if BYTE is LOW. Hi-Z when $\overline{\text{CS}}$ is HIGH and/or R/$\overline{\text{C}}$ is LOW.
12	D4	O	Data Bit 0 (LSB) if BYTE is HIGH. Data bit 8 if BYTE is LOW. Hi-Z when $\overline{\text{CS}}$ is HIGH and/or R/$\overline{\text{C}}$ is LOW.
13	D3	O	LOW if BYTE is HIGH. Data bit 7 if BYTE is LOW. Hi-Z when $\overline{\text{CS}}$ is HIGH and/or R/$\overline{\text{C}}$ is LOW.
14	DGND		Digital Ground
15	D2	O	LOW if BYTE is HIGH. Data bit 6 if BYTE is LOW. Hi-Z when $\overline{\text{CS}}$ is HIGH and/or R/$\overline{\text{C}}$ is LOW.
16	D1	O	LOW if BYTE is HIGH. Data bit 5 if BYTE is LOW. Hi-Z when $\overline{\text{CS}}$ is HIGH and/or R/$\overline{\text{C}}$ is LOW.
17	D0	O	LOW if BYTE is HIGH. Data bit 4 if BYTE is LOW. Hi-Z when $\overline{\text{CS}}$ is HIGH and/or R/$\overline{\text{C}}$ is LOW.
18	DATACLK	I/O	Data Clock Output when EXT/$\overline{\text{INT}}$ is LOW. Data clock input when EXT/$\overline{\text{INT}}$ is HIGH.
19	SDATA	O	Serial Output Synchronized to DATACLK
20	TAG	I	Serial Input When Using an External Data Clock
21	BYTE	I	Selects 8 most significant bits (LOW) or 4 least significant bits (HIGH) on parallel output pins.
22	R/$\overline{\text{C}}$	I	With $\overline{\text{CS}}$ LOW and $\overline{\text{BUSY}}$ HIGH, a Falling Edge on R/$\overline{\text{C}}$ Initiates a New Conversion. With $\overline{\text{CS}}$ LOW, a rising edge on R/$\overline{\text{C}}$ enables the parallel output.
23	$\overline{\text{CS}}$	I	Internally OR'ed with R/$\overline{\text{C}}$. If R/$\overline{\text{C}}$ is LOW, a falling edge on $\overline{\text{CS}}$ initiates a new conversion. If EXT/$\overline{\text{INT}}$ is LOW, this same falling edge will start the transmission of serial data results from the previous conversion.
24	$\overline{\text{BUSY}}$	O	At the start of a conversion, $\overline{\text{BUSY}}$ goes LOW and stays LOW until the conversion is completed and the digital outputs have been updated.
25	PWRD	I	PWRD HIGH shuts down all analog circuitry except the reference. Digital circuitry remains active.
26	REFD	I	REFD HIGH shuts down the internal reference. External reference will be required for conversions.
27	V_{ANA}		Analog Supply. Nominally +5V. Decouple with 0.1µF ceramic and 10µF tantalum capacitors.
28	V_{DIG}		Digital Supply. Nominally +5V. Connect directly to pin 27. Must be ≤ V_{ANA}.

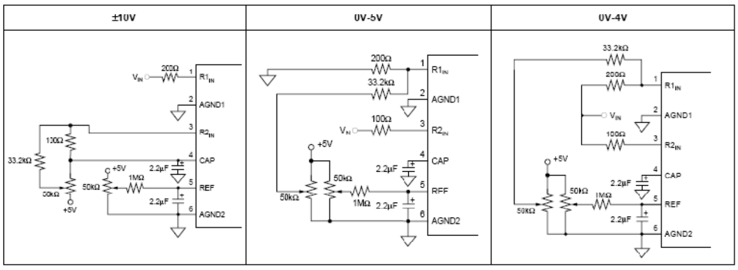


FIGURE 7a. Circuit Diagrams (With Hardware Trim).

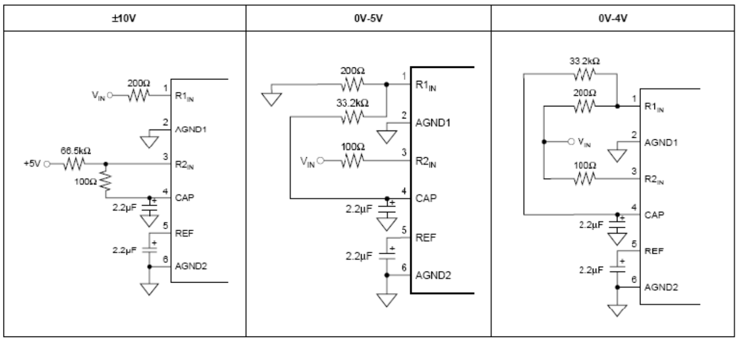


FIGURE 7b. Circuit Diagrams (Without Hardware Trim).

PARAMETER	CONDITIONS	ADS7806P, U MIN	ADS7806P, U TYP	ADS7806P, U MAX	ADS7806PB, UB MIN	ADS7806PB, UB TYP	ADS7806PB, UB MAX	UNITS
RESOLUTION				12			*	Bits
ANALOG INPUT								
Voltage Ranges				±10, 0 to +5, 0 to +4				V
Impedance				(See Table I)				
Capacitance			35			*		pF
THROUGHPUT SPEED								
Conversion Time				20			*	µs
Complete Cycle	Acquire and Convert			25			*	µs
Throughput Rate		40			*			kHz
DC ACCURACY								
Integral Linearity Error			±0.15	±0.9		*	±0.45	LSB(1)
Differential Linearity Error			±0.15	±0.9		*	±0.45	LSB
No Missing Codes			Tested			*		Bits
Transition Noise(2)			0.1			*		LSB
Gain Error			±0.2			±0.1		%
Full-Scale Error(3,4)				±0.5			±0.25	%
Full-Scale Error Drift			±7			±5		ppm/°C
Full-Scale Error(3,4)	Ext. 2.5000V Ref			±0.5			±0.25	%
Full-Scale Error Drift	Ext. 2.5000V Ref		±0.5			*		ppm/°C
Bipolar Zero Error(3)	±10V Range			±10			*	mV
Bipolar Zero Error Drift	±10V Range		±0.5			*		ppm/°C
Unipolar Zero Error(3)	0V to 5V, 0V to 4V Ranges			±3			*	mV
Unipolar Zero Error Drift	0V to 5V, 0V to 4V Ranges		±0.5			*		ppm/°C
Recovery Time to Rated Accuracy from Power-Down(5)	2.2µF Capacitor to CAP		1			*		ms
Power-Supply Sensitivity ($V_{DIG} = V_{ANA} = V_S$)	$+4.75V < V_S < +5.25V$			±0.5			*	LSB

- 12 bits is 1/4096

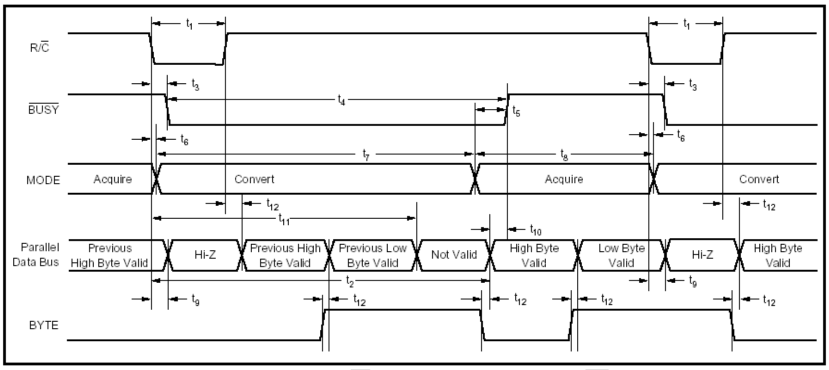
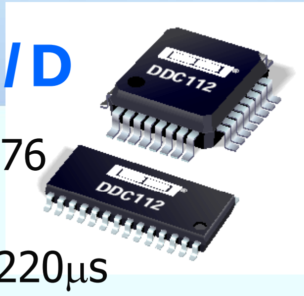


FIGURE 2. Conversion Timing with Parallel Output (CS and DATACLK tied LOW, EXT/INT tied HIGH).

DDC112 Integrating A/D

- 20 bits is 1/1,048,576 = 0.000001
- Conversion time is 220μs



- MONOLITHIC CHARGE MEASUREMENT A/D CONVERTER
- DIGITAL FILTER NOISE REDUCTION: 3.2ppm, rms
- INTEGRAL LINEARITY: ±0.005% Reading ±0.5ppm FSR
- HIGH PRECISION, TRUE INTEGRATING FUNCTION
- PROGRAMMABLE FULL-SCALE
- SINGLE SUPPLY
- CASCADABLE OUTPUT

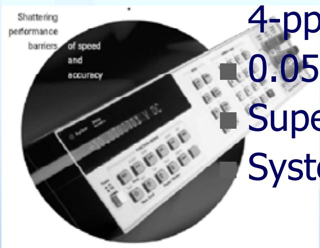
DDC112 Data sheet

PARAMETER	CONDITIONS	DDC112U, Y			DDC112UK, YK			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUTS								
External, Positive Full-Scale								
Range 0	C_{EXT} = 250pF			1000			*	pC
Internal, Positive Full-Scale								
Range 1		47.5	50	52.5	*	*	*	pC
Range 2		95	100	105	*	*	*	pC
Range 3		142.5	150	157.5	*	*	*	pC
Range 4		190	200	210	*	*	*	pC
Range 5		237.5	250	262.5	*	*	*	pC
Range 6		285	300	315	*	*	*	pC
Range 7		332.5	350	367.5	*	*	*	pC
Negative Full-Scale Input		–0.4% of Positive FS				*		pC
DYNAMIC CHARACTERISTICS								
Conversion Rate				2			3	kHz
Integration Time, T_{INT}	Continuous Mode	500		1,000,000	333.3		*	μs
Integration Time, T_{INT}	Non-Continuous Mode	50			*			μs
System Clock Input (CLK)		1	10	12	*	*	15	MHz
Data Clock (DCLK)				12			15	MHz
ACCURACY								
Noise, Low-Level Current Input[1]	C_{SENSOR}[2] = 0pF, Range 5 (250pC)		3.2			*		ppm of FSR[3], rms
	C_{SENSOR} = 25pF, Range 5 (250pC)		3.8			*		ppm of FSR, rms
	C_{SENSOR} = 50pF, Range 5 (250pC)		4.2	6.0		*	7	ppm of FSR, rms
Differential Linearity Error		±0.005% Reading ±0.5ppm FSR (max)					*	
Integral Linearity Error[4]		±0.005% Reading ±0.5ppm FSR (typ)				*		

DDC112 Data sheet (cont.)

	C_{SENSOR} = 50pF, Range 5 (250pC)		4.2	6.0		*	7	ppm of FSR, rms
Differential Linearity Error			±0.005% Reading ±0.5ppm FSR (max)				*	
Integral Linearity Error[4]			±0.005% Reading ±0.5ppm FSR (typ)			*		
			±0.025% Reading ±1.0ppm FSR (max)				*	
No Missing Codes			20			*		Bits
Input Bias Current	T_A = +25°C		0.1	10		*	*	pA
Range Error	Range 5 (250pC)			5			*	% of FSR
Range Error Match[5]	All Ranges		0.1	0.5		*	*	% of FSR
Range Sensitivity to V_{REF}	V_{REF} = 4.096 ±0.1V		1:1			*		
Offset Error	Range 5, (250pC)		±200			*	±600	ppm of FSR
Offset Error Match[5]			±100			*		ppm of FSR
DC Bias Voltage[6] (Input V_{OS})			±0.05	±2		*	*	mV
Power-Supply Rejection Ratio			±25	±200		*	*	ppm of FSR/V
Internal Test Signal			13			*		pC
Internal Test Accuracy			±10			*		%
PERFORMANCE OVER TEMPERATURE								
Offset Drift			±0.5				±3[10]	ppm of FSR/°C
Offset Drift Stability			±0.2			*	±0.7[10]	ppm of FSR/minute
DC Bias Voltage Drift	Applied to Sensor Input		3			±1		µV/°C
Input Bias Current Drift	+25°C to +45°C		0.01	1[10]		*	*	pA/°C
Input Bias Current	T_A = +75°C		2	50[10]		*	*	pA
Range Drift[7]	Range 5 (250pC)		25		0	25	50[10]	ppm/°C
Range Drift Match[5]	Range 5 (250pC)		±0.05			*		ppm/°C
REFERENCE								
Voltage		4.000	4.096	4.200	*	*	*	V
Input Current[8]	T_{INT} = 500µs		150			225	275	µA
DIGITAL INPUT/OUTPUT								

Agilent 3458A



- Measurement Capability
  - 8-ppm 1 year dcV accuracy, optional 4-ppm
  - 0.05 ppm dcV transfer accuracy
  - Superior AC voltage measurements
- System Capability
  - 100,000 readings per second at 4 1/2 digits
- US$ 7,892

www.agilent.com

dc Volts
- 5 ranges: 0.1 V to 1000 V
- 8.5 to 4.5 digit resolution
- Up to 100,000 readings/sec (4.5 digits)
- Maximum sensitivity: 10 nV
- 0.6 ppm 24 hour accuracy
- 8 ppm (4 ppm optional) / year voltage reference stability

Ohms
- 9 ranges: 10 Ω to 1GΩ
- Two-wire and four-wire Ohms with offset compensation
- Up to 50,000 readings/sec (5.5 digits)
- Maximum Sensitivity: 10μΩ
- 2.2 ppm 24 hour accuracy

ac Volts
- 6 ranges: 10 mV to 1000 V
- 1 Hz to 10 MHz bandwidth
- Up to 50 readings/sec with all readings to specified accuracy
- Choice of sampling or analog true rms techniques
- 100 ppm best accuracy

dc Current
- 8 ranges: 100 nA to 1 A
- Up to 1,350 readings/sec (5.5digits)
- Maximum sensitivity: 1pA
- 14 ppm 24 hour accuracy

ac Current
- 5 ranges: 100 μA to 1 A
- 10Hz to 100 kHz bandwidth
- Up to 50 readings/sec
- 500 ppm 24 hour accuracy

Frequency and period
- Voltage or current ranges
- Frequency: 1 Hz to 10 MHz
- Period: 100 ns to 1 sec
- 0.01% accuracy
- ac or dc coupled

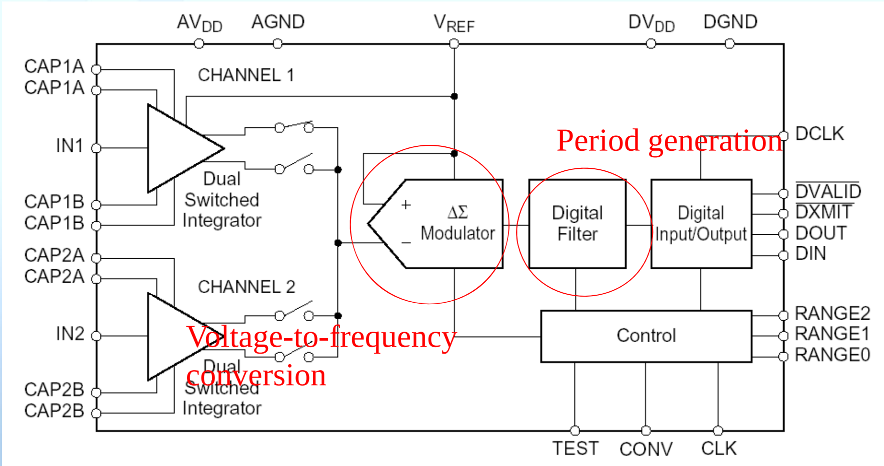
Maximum speeds
- 100,000 readings/sec at 4.5 digits (16 bits)
- 50,000 readings/sec at 5.5 digits
- 6,000 readings/sec at 6.5 digits
- 60 readings/sec at 7.5 digits
- 6 readings/sec at 8.5 digits

Measurement set-up speed
- 100,000 readings/sec over GPIB or with internal memory
- 110 autoranges/sec
- 340 function or range changes/sec
- Post-processed math from internal memory

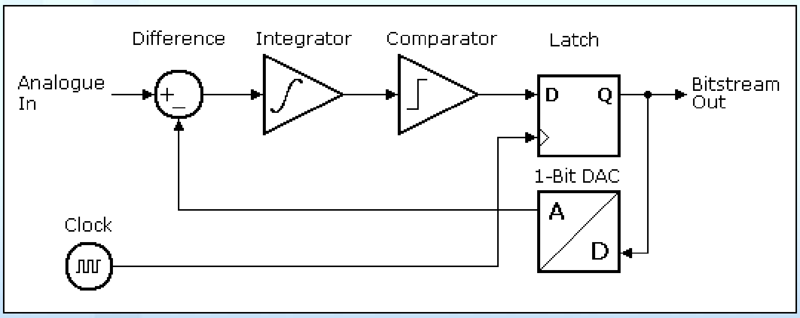
ΔΣ Converter

- Converting amplitude into frequency
- Utilizing the fast clock rate in modern IC
- Achieving fast conversion with high resolution
- Scalable compromise between resolution and speed
- Low operating voltage
- Example TI ADS7806

Charge-Digitizing A / D

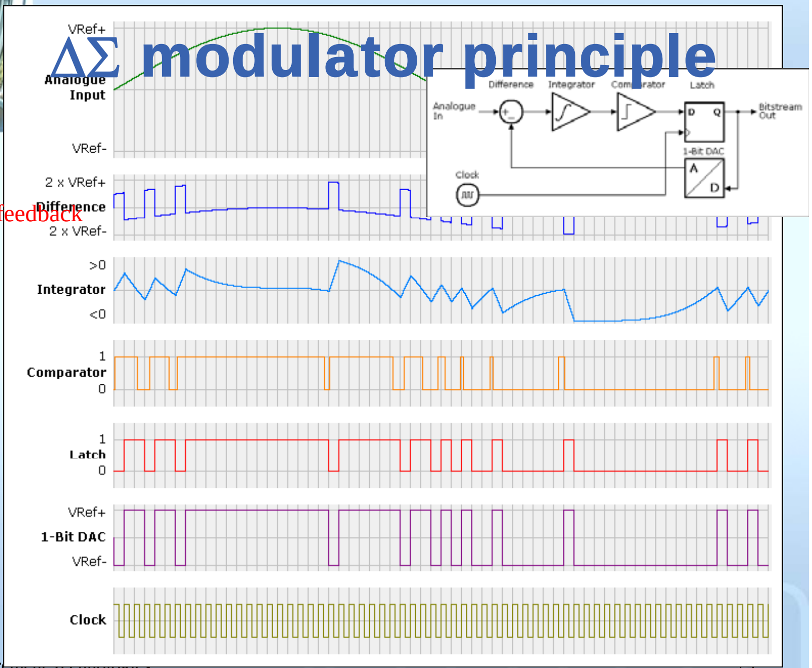


First order delta-sigma modulator



ΔΣ modulator principle

Difference from 1-bit feedback



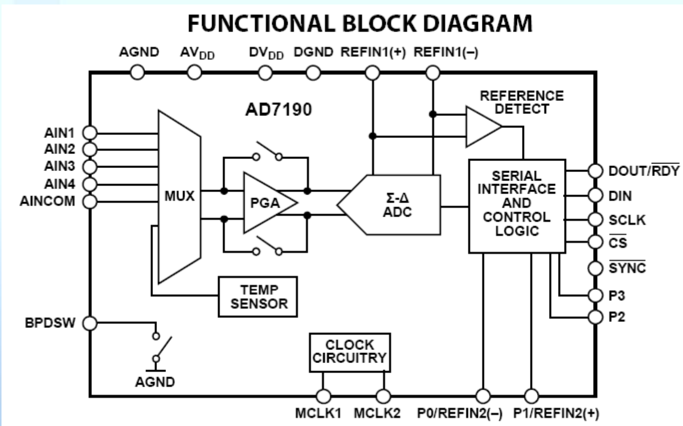
Analog Device AD7190

- GENERAL DESCRIPTION
- Low noise, complete analog front end for high precision measurement applications. It contains a low noise, 24-bit sigma-delta (Σ-Δ) analog to digital converter (ADC). **On-Chip** low noise gain stage allow **signals of small amplitude can be interfaced directly to the ADC**.
- **Two differential inputs** or **four pseudo differential inputs**. The on-chip channel sequencer allows several channels to be enabled, and the AD7190 **sequentially converts** on each **enabled** channel. This simplifies communication with the part. The on-chip 4.92 MHz clock can be used as the clock source to the ADC or, alternatively, an external clock or crystal can be used. The output data rate from the part can be varied from 4.7 Hz to 4.8 kHz.
- **Two digital filter options**. The choice of filter affects the rms noise/noise-free resolution at the programmed output data rate, the settling time, and the 50 Hz/60 Hz rejection. For applications that require all conversions to be settled, the AD7190 includes a zero latency feature.
- **Operates with 5 V analog power supply** and a digital power supply from 2.7 V to 5.25 V. It consumes a current of 6 mA. It is housed in a 24-lead TSSOP package.

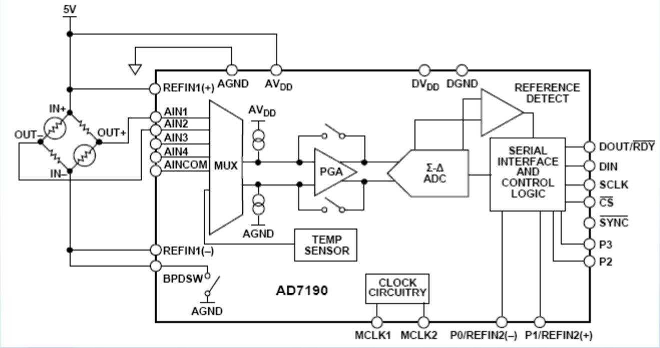
Analog Device AD7190

- FEATURES
  - RMS noise: 8.5 nV @ 4.7 Hz (gain = 128)
  - **16 noise free bits** @ 2.4 kHz (gain = 128)
  - **Up to 22.5 noise free bits** (gain = 1)
  - Offset drift: 5 nV/°C
  - Gain drift: 1 ppm/°C
  - Specified drift over time
  - 2 differential/4 pseudo differential input channels
  - Automatic channel sequencer
  - Programmable gain (1 to 128)
  - Output data rate: 4.7 Hz to 4.8 kHz
  - Internal or external clock
  - Simultaneous 50 Hz/60 Hz rejection
  - 4 general-purpose digital outputs
  - Power supply
  - AVDD: 4.75 V to 5.25 V
  - DVDD: 2.7 V to 5.25 V
  - Current: 6 mA
  - Temperature range: –40°C to +105°C
  - Interface
  - 3-wire serial
  - SPI, QSPI™, MICROWIRE™, and DSP compatible
  - Schmitt trigger on SCLK
- APPLICATIONS
  - Weigh scales
  - Strain gauge transducers
  - Pressure measurement
  - Temperature measurement

AD7190 block diagram

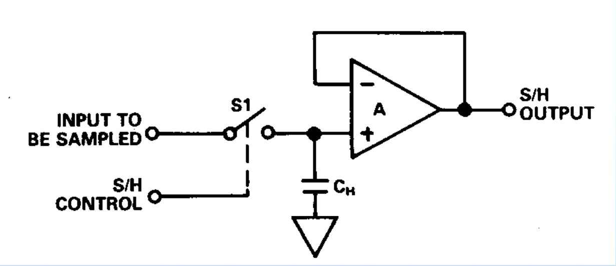


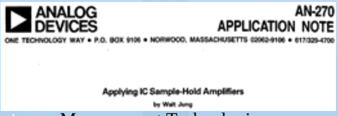
AD7190 application example



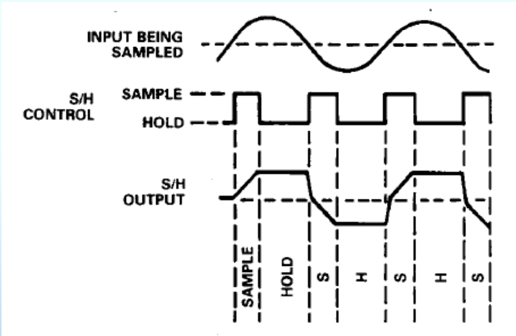
Sample and Hold

- Sample and hold block diagram





Sample and hold waveform

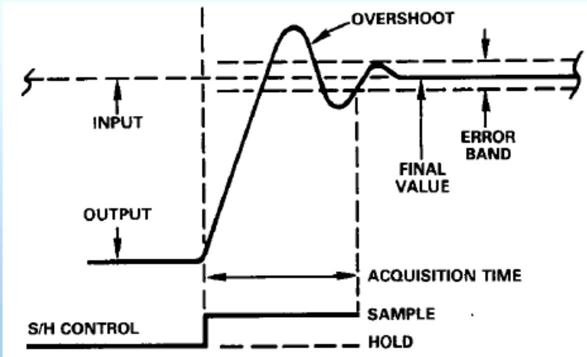


Practical Sample and Hold

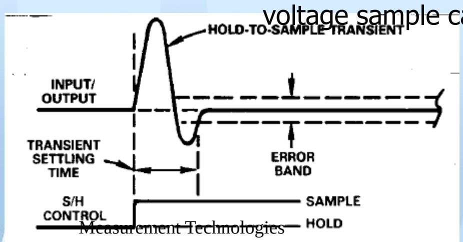
- Hold-to-sample transition
- Sample interval
- Sample-to-hold transition
- Hold interval

Hold-to-sample transition errors

- Acquisition time – time required for the S/H to acquire and than track the input signal after the "sample" commend.



- Hold-to-sample mode transient, and settling time
  - This transient will be present even in the case where there is no large difference between the previously held voltage and the new sample.
  - The amplitude of this transient may be well in excess of the rated S/H accuracy, it must be allowed a sufficient time period to die out before the output voltage sample can be considered valid.



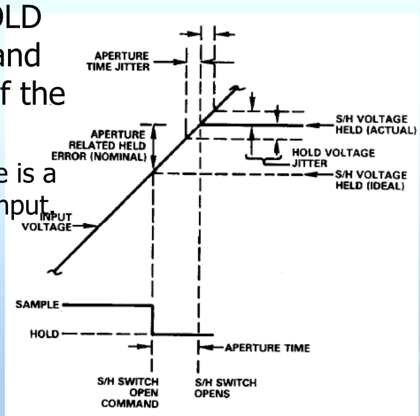
Sample errors

- Gain nonlinearity
- Offset
- Offset temperature drift
- Settling time

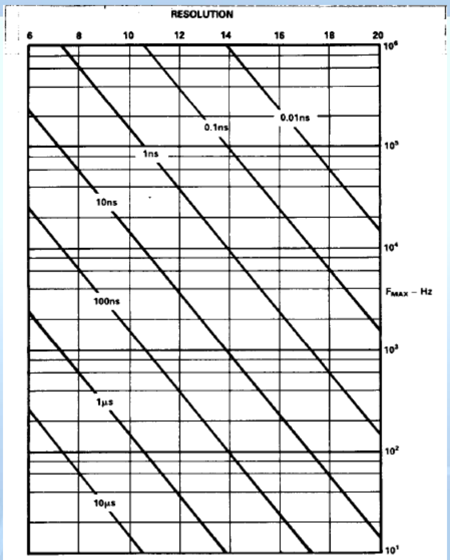
Sample-to-hold transition errors

- Aperture time
- S/H offset

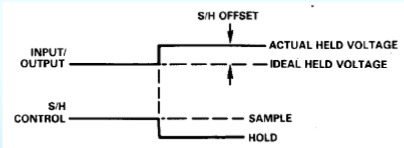
- Aperture time - The time which elapses between the point when a HOLD command is issued and the actual opening of the S/A switch.
  - Problem!! when there is a rapid change in the input.
- Aperture related time/voltage errors



- Maximum input sine wave frequency for various aperture times and resolutions



- S/H offset

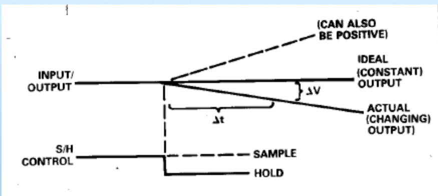


- Sample-to-hold settling time –
  - The time for the S/H output to settle to within its rated accuracy following the Hold command.

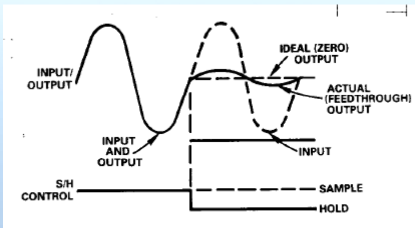
Hold Interval Errors

$\Delta V / \Delta t = I_L / C_H$

- Where
- I_L is the leakage current
- C_H is the Hold capacitor value



- Feedthrough
  - Is an analog error caused by leakage of ac signals through the S/H switch in the HOLD state.



Dielectric Absorption

- With some common capacitor types, the dielectric does not completely release all of its energy after a charge/discharge cycle.

Drift and Noise

- A S/H can possess different drift characteristics in the HOLD mode than those in the SAMPLE mode.
  - In the HOLD mode, the output terminal sees only the drift of the output buffer amplifier.
  - In the SAMPLE mode, it sees either the input amplifier alone or the composite drift of two series amplifiers.